IN THE CLAIMS

Kindly cancel, without prejudice, claim 18.

1 (previously presented): A method of designing a clock tree in an integrated circuit, comprising the steps of:

collecting a set of sink locations in a master list and a set of blocked areas;

(a) selecting a temporary insertion point (TIP);

(b) enclosing a sink at a first level farthest from the TIP in a bin that includes a first subset of sinks and remove the first subset of sinks from the master list;

(c) assigning a first-level structured clock buffer (SCB) to the bin, in which said step (c) of assigning a first-level SCB to the bin comprises the steps of attempting to place a horizontal SCB, then attempting to place a vertical SCB in a central location when a horizontal SCB will not fit in said central location;

repeating steps (a), (b) and (c) above for the remaining sinks in the first level of buffers and subsequent levels until a root level is reached;

improving the symmetry of the tree by moving the SCB locations within constraints to concentrate SCBs in rows and columns;

connecting the root level TIP to lower levels; and

connecting a source (S) of clock signals to the root level TIP.

2-10 (canceled)

11 (previously presented): The method as claimed in claim 1, in which said step (a) of selecting a TIP comprises calculating a center of sinks and a centroid of sinks and automatically placing said TIP at one of said center, centroid or an intermediate point between said center and centroid in accordance with an algorithm that locates available space.

12 (previously presented): The method as claimed in claim 1, in which said step (a) of selecting a TIP comprises calculating a center of sinks and a centroid of sinks and

automatically placing said TIP at one of said center, centroid or an intermediate point between said center and centroid in accordance with an algorithm that locates and selectively weights one or more of delay, power consumed and placability.

13 (previously presented): The method as claimed in claim 1, in which said vertical SCB comprises a set of circuit elements laid out to have substantially the same delay as a corresponding SCB with horizontal layout.

14 (previously presented): The method as claimed in claim 1, in which said step of improving the symmetry comprises a step of calculating for each of a set of columns and rows a potential improvement in symmetry of SCBs in an nth level of said tree and moving SCBs to improve symmetry.

15 (previously presented): The method as claimed in claim 14, in which some designated SCBs are excluded from the calculation in said step of improving the symmetry, whereby only a subset of SCBs is included in the calculation.

16 (previously presented): The method as claimed in claim 14, in which the amount of movement permitted to improve symmetry is restricted to a preset amount.

17 (previously presented): The method as claimed in claim 1, in which said SCB assigned to a subset of sinks is selected from a set of predesigned SCBs of varying capacity.

18 (canceled) An article of manufacture comprising a computer readable storage medium which contains a set of instructions for performing a method according to claim 1.